Chapter 7
Building Blocks of Integrated Circuit Amplifiers:

Part A: Comparison of MOSFET and BJT
Comparison: MOSFET and BJT

NMOS

PMOS

D: Drain
G: Gate
S: Source

C: Collector
B: Base
E: Emitter
Comparison: MOSFET and BJT

**NMOS**

- Source region
- Channel region
- Drain region
- p-type substrate (Body)
- Oxide (SiO₂)

**NPN**

- Emitter (E)
- Base (B)
- Collector (C)
- p-type substrate (Body)
- Collector-base junction (CBJ)
- Emitter-base junction (EBJ)
- n-type
- p

NMOS Basics: Micro I 01Chapter 5-1.ppt, Slides 13-15

NPN Basics: Micro I 01Chapter 6-1.ppt, Slides 8-11
Comparison: MOSFET and BJT

- Popular in IC design
- Low current driving capability
- MOSFETs have to be tailored for harsh environments: not common
- Significant parasitic effect at very high frequencies
- MOSFETs have higher $1/f$ (flicker noise) but lower thermal noise
- MOSFETs are symmetrical: source and drain are interchangeable (while designing an IC)

- Popular in discrete design
- High current driving capability
- BJTs are more robust: can operate in severe environmental conditions
- Good performance at very high frequencies (GHz range*)
- BJTs have lower $1/f$ (flicker noise) but higher thermal noise
- BJTs are not symmetrical: EBJ (emitter to base junction) is fixed and can only be operated in specific way

* These devices are called Heterojunction Bipolar Transistors (HBT); they have high gain and low noise at frequencies in the order of several hundred GHz
# Modes of Operation

## Amplifier

<table>
<thead>
<tr>
<th>Mode</th>
<th>$v_{GS}$</th>
<th>$v_{DS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>$v_{GS} &lt; V_{tn}$</td>
<td>-</td>
</tr>
<tr>
<td>Triode</td>
<td>$v_{GS} &gt; V_{tn}$</td>
<td>$v_{DS} &lt; v_{OV}$</td>
</tr>
<tr>
<td>Saturation</td>
<td>$v_{GS} &gt; V_{tn}$</td>
<td>$v_{DS} &gt; v_{OV}$</td>
</tr>
</tbody>
</table>

See Table 7.A.3

## Amplifier

### EBJ
- Cutoff: Reverse
- Active: Forward
- Saturation: Reverse

### CBJ
- Cutoff: Reverse
- Active: Forward
- Saturation: Forward

See Table 7.A.3
### Biasing Requirements

#### NMOS

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</table>

1. **Induce a channel:**
   
   $v_{GS} \geq V_{t}$, \hspace{1cm} $V_{t} = 0.3 - 0.5 \text{ V}$
   
   Let $v_{GS} = V_{t} + v_{OV}$

2. **Pinch-off channel at drain:**
   
   $v_{GD} < V_{t}$
   
   or equivalently,
   
   $v_{DS} \geq V_{OV}$, \hspace{1cm} $V_{OV} = 0.1 - 0.3 \text{ V}$

<table>
<thead>
<tr>
<th>$i_D =$</th>
<th>$i_G =$</th>
</tr>
</thead>
</table>

#### NPN

<table>
<thead>
<tr>
<th>Mode</th>
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<th>CBJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>Reverse</td>
<td>Reverse</td>
</tr>
<tr>
<td>Active</td>
<td>Forward</td>
<td>Reverse</td>
</tr>
<tr>
<td>Saturation</td>
<td>Forward</td>
<td>Forward</td>
</tr>
</tbody>
</table>

1. **Forward-bias EBJ:**
   
   $v_{BE} \geq V_{BEon}$, \hspace{1cm} $V_{BEon} \approx 0.5 \text{ V}$

2. **Reverse-bias CBJ:**
   
   $v_{BC} < V_{BCon}$, \hspace{1cm} $V_{BCon} \approx 0.4 \text{ V}$
   
   or equivalently,
   
   $v_{CE} \geq 0.3 \text{ V}$

<table>
<thead>
<tr>
<th>$i_C =$</th>
<th>$i_B =$</th>
</tr>
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How does the transistor amplify signals?

Voltage Transfer Curve (VTC)
Above behavioral models show that, when a small signal is applied to Gate (Base), Drain (Collector) will produce a large signal.
Small Signal Models: High Frequency

NMOS

See Table 9.1

NPN

See Table 9.1
FYI: Fabrication of MOSFET

NMOS Layout (Masks): Top View

- Metal (Gate Connection)
- Metal (Drain Connection)
- Via (contact)
- Polysilicon (Gate)
- NWELL
- PWELL
- Active Region (green)
- Body Contact (Not Always Grounded)
- NMOS
- Metal (Source Connection)
- S
- D
- gnd
FYI: Fabrication of MOSFET

NMOS Layout: 3D Side Views
CS and CE Amplifiers

CS (Common Source) Amplifier

CE (Common Emitter) Amplifier