Lecture 11

Phase Locked Loop (PLL): Appendix C
Digital Communication System

- Information (sound, video, text, data, ...)
- Transducer & A/D Converter
- Source Encoder
- Channel Encoder
- Modulator
- Tx RF System
- Channel
- Rx RF System
- Output Signal
- D/A Converter and/or output transducer
- Source Decoder
- Channel Decoder
- Demodulator
PLL: Core Component for the Receiver

Example: AM Radio

Transmitter

Receiver

Phase Locked Loop (PLL) is used to get the precise frequency

Same Frequency As the Carrier Signal
PLL: Core Component for the Receiver

Super Heterodyne Receiver

Phase Locked Loop (PLL) is used to get the precise frequency
PLL: Core Component for the Receiver

Zero IF or Direct Conversion Receiver

Phase Locked Loop (PLL) is used to get the precise frequency
Continuous-time PLL Basics

- PLL a device that tracks phase and frequency of a sinusoid signal and provides the stable **reference signal**
- PLL has three main components: Phase Detector (PD), Loop Filter (LF), and Voltage Controlled Oscillator (VCO)

![Continuous-time PLL Diagram]

\[
\hat{\theta}(t) = k_0 \int_{-\infty}^{t} v(x) \, dx
\]
Continuous-time PLL Basics

- **Stable Frequency**: once the VCO phase is “locked” or “synchronized” (i.e. phase difference is constant) to the received signal, its frequency is said to be “locked”
- Consider two sinusoids (points) around the unit circle
- If the phase difference between the two is constant, then they move around at the same rate (same frequency $\omega$)

Ref: [Phase Locked Loop PLL Tutorial](https://example.com/phase-locked-loop)
**Continuous-time PLL Basics**

- **Stable Frequency**: once the VCO phase is “locked” or “synchronized” (phase difference is constant) to the received signal, its frequency is locked.
- **Stable Phase**: minimize the phase error between the received signal phase $\theta(t)$ and the VCO signal phase $\hat{\theta}(t)$.
- Phase Detector (PD): finds the phase difference (phase error), $\theta_e(t) = \theta(t) - \hat{\theta}(t)$.
- Loop Filter (LF): filters out phase error and produces control voltage $v(t)$.
- Voltage Controlled Oscillator (VCO): generates the reference signal.

![Continuous-time PLL Diagram](image)
Ideal Operation

*Loop adjusts the control voltage \( v(t) \) of VCO until phase error,
\[ \theta(t) - \hat{\theta}(t) \approx 0 \]

1) \( \theta(t) > \hat{\theta}(t) \): VCO output lags the carrier signal
   - Loop filter will generate \( v(t) > 0 \) so that \( \hat{\theta}(t) \) increases

2) \( \theta(t) < \hat{\theta}(t) \): VCO output leads the carrier signal
   - Loop filter will generate \( v(t) < 0 \) so that \( \hat{\theta}(t) \) decreases
Phase Equivalent Representation

Loop adjusts control voltage of VCO until phase error $\sim 0$

$\theta(t)$ 

Phase Detector 

$g(\cdot)$ 

Loop Filter 

$F(s)$ 

Received Signal Phase 

Reference Signal Phase 

$\hat{\theta}(t)$ 

$\int_{-\infty}^{t} (\cdot) \, dx$ 

$VCO$ 

$\nu(t)$
Continuous-time PLL Basics

- Time and Frequency Domain Representation

*Loop adjusts control voltage of VCO until phase error ~ 0*

- Loop Transfer Function:

\[
H_a(s) = \frac{\hat{\Theta}(s)}{\Theta(s)} = \frac{k_0 k_p F(s)}{s + k_0 k_p F(s)}
\]

- Phase Error Transfer Function:

\[
G_a(s) = \frac{\Theta_e(s)}{\Theta(s)} = \frac{s}{s + k_0 k_p F(s)}
\]

**Diagram:**

- Time-Domain
- Frequency-Domain (Laplace T.)
Phase Error Transfer Function

Phase Error Transfer Function:

\[ G_a(s) = \frac{\Theta_e(s)}{\Theta(s)} = \frac{s}{s + k_0 k_p F(s)} \]

We need to come up with \( F(s) \) or the Loop Filter

Two cases:

**Phase Offset (step input)**

- \( \omega_0 t + \Delta \theta u(t) \)
- Multipath Delay

**Frequency Offset (ramp input)**

- \( \omega_0 t + (\Delta \omega) t u(t) \)
- L.O. Frequency Instability
## Loop Filter, $F(s)$

- **Sections C.1.2, C.1.3, C.1.4**

### Table C.1.1: Summary of loop filter characteristics and steady-state phase errors

<table>
<thead>
<tr>
<th>$F(s)$</th>
<th>$F(0)$</th>
<th>$\theta_{e,\text{step}}(\infty)$</th>
<th>$\theta_{e,\text{ramp}}(\infty)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k$</td>
<td>$k$</td>
<td>0</td>
<td>$\frac{\Delta\omega}{k_0k_pk}$</td>
</tr>
<tr>
<td>$\frac{k}{s+k}$</td>
<td>1</td>
<td>0</td>
<td>$\frac{\Delta\omega}{k_0k_p}$</td>
</tr>
<tr>
<td>$k_1 + \frac{k_2}{s}$</td>
<td>$\infty$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$\frac{k_1+s}{k_2+s}$</td>
<td>$k_1$</td>
<td>0</td>
<td>$\frac{\Delta\omega k_2}{k_0k_pk_1}$</td>
</tr>
</tbody>
</table>

- **Phase Lock**
- **Frequency Lock**

**The best Loop Filter is Proportional-Plus- Integrator**
Loop Filter, $F(s)$

- Sections C.1.2, C.1.3, C.1.4

Table C.1.3 Transfer function, loop parameters, and equivalent noise bandwidth for a phase locked loop using the four loop filters of interest

<table>
<thead>
<tr>
<th>Loop Filter $F(s)$</th>
<th>$\zeta$</th>
<th>$\omega_n$</th>
<th>$H_a(s)$</th>
<th>$B_n$ (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k$</td>
<td>–</td>
<td>–</td>
<td>$\frac{k_0k_pk}{s+k_pk_0k}$</td>
<td>$\frac{k_0k_pk}{4}$</td>
</tr>
<tr>
<td>$\frac{k}{k+s}$</td>
<td>$\frac{1}{2}\sqrt{\frac{k}{k_0k_p}}$</td>
<td>$\sqrt{k_0k_pk}$</td>
<td>$\frac{\omega_n^2}{s^2 + 2\zeta\omega_ns + \omega_n^2}$</td>
<td>$\frac{\omega_n}{8\zeta}$</td>
</tr>
<tr>
<td>$\frac{k_1 + k_2}{s}$</td>
<td>$\frac{k_1}{2}\sqrt{\frac{k_0k_p}{k_2}}$</td>
<td>$\sqrt{k_0k_pk_2}$</td>
<td>$\frac{2\zeta\omega_ns + \omega_n^2}{s^2 + 2\zeta\omega_ns + \omega_n^2}$</td>
<td>$\frac{\omega_n}{2 \left( \frac{1}{4\zeta} + \zeta \right)}$</td>
</tr>
<tr>
<td>$\frac{k_1 + s}{k_2 + s}$</td>
<td>$\frac{1}{2}\frac{k_0k_p + k_2}{\sqrt{k_0k_pk_1}}$</td>
<td>$\sqrt{k_0k_pk_1}$</td>
<td>$\frac{\omega_n^2 + \omega_n \left( 2\zeta - \frac{k_2}{\omega_n} \right)}{s^2 + 2\zeta\omega_ns + \omega_n^2}$</td>
<td>$\frac{\omega_n}{8\zeta} \left[ 1 + \left( 2\zeta - \frac{k_2}{\omega_n} \right)^2 \right]$</td>
</tr>
</tbody>
</table>

Loop Filter has $p$ poles, the PLL has $p+1$ poles
Loop Filter Characteristics

1) Acquisition Time or Locking Time: time required to make phase error=0

\[ T_{LOCK} = T_{FL} + T_{PL}; \]

\[ T_{FL} = 4 \frac{\Delta f^2}{B_n^3} \]

\[ T_{PL} = 1.3 \frac{B_n}{B_n} \]

- Frequency Offset
- Noise Bandwidth (or PLL Bandwidth)

Pull-in Range: \( \Delta f_{\text{pull-in}} = (2\pi\sqrt{2}\zeta)B_n \)

2) Tracking:

Q: How well can the PLL track the carrier signal?

A: Phase error variance

\[ \sigma_{\theta_e}^2 = \frac{N_0B_n}{P_{in}} ; P_{in}=\text{Received sig. power with AWGN with noise} = N_o/2 \]

Trade-off: Fast Acquisition and Good Tracking
Loop Transfer Function

\[ H_a(s) = \frac{2\zeta \omega_n s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \]

Loop Constants

\[ k_0 k_p k_1 = 2\zeta \omega_n; \quad k_0 k_p k_2 = \omega_n^2 \]

Selection of Damping Factor \( \zeta \)
Discrete-time PLL with Proportional-Plus-Integrator LF

Loop Transfer Function

**Eq. C.51**

Loop Constants

**Eq. C.61**

Direct Digital Synthesizer (DDS)

Frequency-Domain (Z-Transform)
Discrete-time PLL Example (Fig. C.2.4)

Goal: Track Complex Exponential

Follow Dr. Rice’s PLL Exercise

Design first-order PLL and second-order PLL
Assignment 7 [10]

- Simulate 1\textsuperscript{st} order and 2\textsuperscript{nd} order discrete-time PLLs [10]

Submit the following:

1) Simulink Model
2) Phase error plots
3) Time-domain plots