EE2700 Tentative Course Schedule – Spring 2014

Date	Reading	Synopsis	Lab/Project
1/6/13	Ch. 1	Syllabus, Lab books, History, Digital Signals	
1/8/13	Ch. 2	Binary Representation, Lab 1	L1. Digital I/O
1/13/13	Ch. 3, 4.1	Digital Input and Output, Boolean Algebra	
1/15/13	Ch. 4.2	Properties, Theorems, Truth Tables, Minterms, Lab 2	L2. Inverters
1/20/13		Civil Rights Day	
1/22/13	Ch. 5.1-5.3	Logic Design, lab 3	L3. Exclusive OR
1/27/13	Ch. 5.4-5.5	Logic Analysis, Implementation, Tri-state, open drain	
1/29/13	Ch. 6.1-6.6	Standard Logic Chips. Lab 4	L4. Comparitor
2/3/13	Ch. 7.1-7.2	Karnaugh Maps, don't-cares	
2/5/13	Ch. 8	Design Process, binary arithmetic, Lab 5	L5. 1-bit Full Adder
2/10/13	Ch. 7.2-7.4	Variable Entered Maps, Review for Exam	
2/12/13		Exam 1 (thru 2/5/13)	Catch-up day
2/17/13		President's Day	
2/19/13		Return exam, ISE Demo - Basic Simulation, Lab 6	L6. 2-bit Full Adder
2/24/13	Ch. 9.1-9.6	VHDL, Behavioral/Structural Models, Test Benches	
2/26/13	Ch. 10	Multiplexers, Codes, Encoders (w/VHDL models)	L6. Continued
3/3/13	Ch. 11	Demultiplexers/Decoders, Comparitors	
3/5/13		Fast Carry Adders, Shifters, Project 1	Project 1
3/10/13		Spring Break	
3/12/13		Spring Break	
3/17/13		Latches, Flip-flops	
3/19/13	Ch. 12	Registers, Counters, Programming CPLDs, Lab 7	L7. CPLD adder
3/24/13		Addressable Memory, Project 2, Exam Review	
3/26/13		Exam 2 (thru 3/19)	Project 2
3/31/13	Ch. 14.1-7	State machines, assignment, implementation, Lab 8	
4/2/13	Ch. 13.1-2	Data path (size reduction, pipelining)	L8. Seq. Finder
4/7/13	Ch. 14.8-12	Controllers, Synchronization, Pulsers, Glitches.	
4/9/13	Ch. 14.9	State Machines in VHDL, Lab 9	L9. Garage Opener
4/14/13		A controller for a simple processor, Project 3	
4/16/13		*Meet in lab to work on Project 3	Project 3
4/21/13		Review for Exam	
4/23/13		Final Exam, 11:00AM	