EE 2700
Digital Circuits

Lab 9 – Garage Door Opener

Objective: In this lab, the student will gain experience by designing a state machine with asynchronous inputs using VHDL and implementing it in a CPLD.

Preparation:

Using the state diagram on the next page, design a controller for a garage door opener in VHDL that has two outputs for the garage door motor, one to drive the door up and the other to drive the door down (both asserted high). There are two stop switches, one that activates when the door is fully open (top) and one that activates when the door is fully closed (bottom). These inputs are asserted (active) low, as is the button input that turns the motor on and off. If the door is closed, the button should make the door go up. If the door is fully open, the button should make the door go down. Otherwise, the door should go in the direction opposite its last movement. Finally, there is a sensor input (also asserted low) that indicates an obstruction. If this signal is asserted while the garage door is going down, the door must immediately (i.e. on the next clock) reverse. Additionally, if the sensor input is asserted when the button is pressed and the motor is stopped, the garage door must be driven upward (unless it is already at the top stop). The clock input is 60Hz. Reset is asserted low.

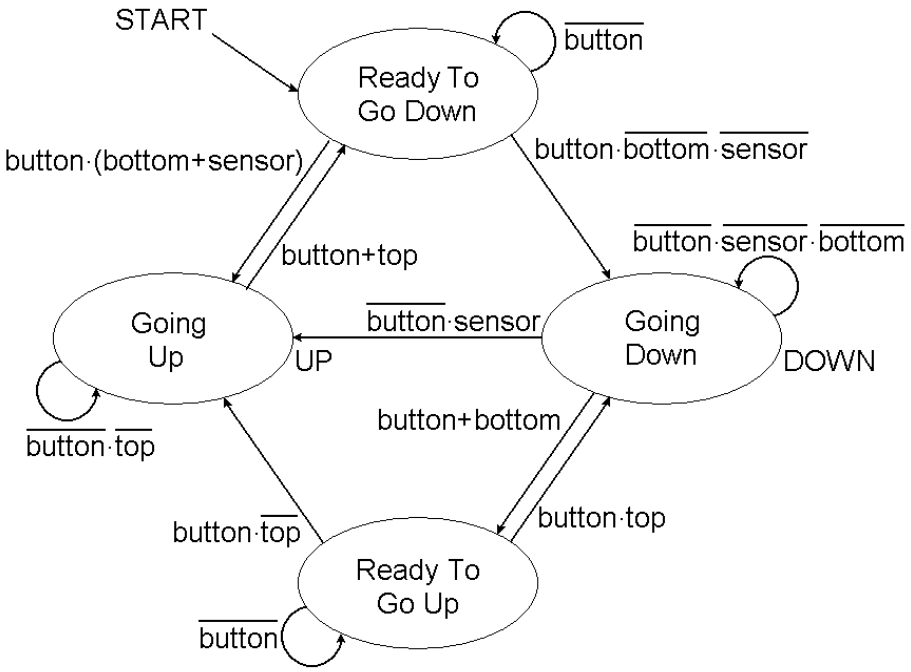
All inputs (except clock and reset) must be synchronized, but the 60Hz clock will make de-bouncing unnecessary. Also, it will be to your advantage to precondition the button signal with a “single pulse” circuit so that it is asserted for one clock period each time the button is pressed.

Design the controller and simulate it extensively. Print your VHDL module, test bench and simulation results and affix them to your lab book.

Create an implementation constraints file for your module and include the following constraints (or something similar):

```
NET "RST_L"    LOC = "P18" | IOSTANDARD = LVCMOS33 ;
NET "TOP_L"    LOC = "P19" | IOSTANDARD = LVCMOS33 ;
NET "BOTTOM_L" LOC = "P20" | IOSTANDARD = LVCMOS33 ;
NET "SENSOR_L" LOC = "P21" | IOSTANDARD = LVCMOS33 ;
NET "BUTTON_L" LOC = "P22" | IOSTANDARD = LVCMOS33 ;
NET "UP"       LOC = "P27" | IOSTANDARD = LVCMOS33 ;
NET "DOWN"     LOC = "P28" | IOSTANDARD = LVCMOS33 ;
NET "CLK"      LOC = "P43" | IOSTANDARD = LVCMOS33 ;
```

Make sure ISE is configured for an XC2C64A in a VQ44 package. Synthesize your design. Remember to configure each pin for pull-ups. (Right-click on the “Fit” process and select process properties.) Create the JEDEC file for your design and copy it to a memory stick. Affix a copy of the implementation constraints file to your lab book.



Parts: All required parts are supplied in the lab.

Procedure: One of the computers in the lab is connected via a USB programming cable to a model garage door. Make sure power (10 Volts) is supplied to the model. Run Adept (installed on the computer) to download your code to the CPLD in the model. After the CPLD is programmed, use the open/close button and the sensor button on the model to test the functionality of your design. Record your results.

Demonstrate the circuit to your lab instructor.

Signoff: A lab score can only be given if the circuit is functional.

Rubric (10 points total)

- Lab book contains a title and description and is clearly legible. (1 point)
- Lab book contains a schematic with chip and pins labeled (1 point)
- Lab book contains the VHDL module and test bench (1 point)
- Lab book contains simulation results (1 point)
- Lab book contains observed test results (1 point)
- Lab book contains no obliterations. (1 point)
- Lab book contains a signed, dated summary (1 point)
- Each used page has a page number and is initialed* and dated* (1 point)
- The circuit is functional before the end of the lab period. (2 points)

Note: If the circuit is working at the end of the lab period but the lab book is not yet complete, the lab can be signed off as “working”, and no late penalty will be assessed if it is graded on or before the next lab period.

* It is not necessary to initial and date a page that contains a signature and date unless the dates are different.